REMARKS

I. Present Status of the Application

The Office Action rejected all presently-pending claims 1-16. Specifically, the Office Action rejected claims 1-4 and 9-12 under 35 U.S.C. 103(a), as being unpatentable over Seal et al. (U.S. 5,583,804). The Office Action further rejected claims 5-8 and 13-16 under 35 U.S.C. 103(a), as being unpatentable over Seal et al. (U.S. 5,583,804), further in view of Morrison et al. (U.S. 6,581,086). In response thereto, Applicants have cancelled claims 1-2 and 9-10. After entry of the foregoing amendments, claims 3-8 and 11-16 remain pending in the present application, and reconsideration of those claims is respectfully requested.

III. Discussion of Office Action Rejection Addressed to Claims 1-4 and 9-12

The Office Action rejected claims 1-4 and 9-12 under 35 U.S.C. 103(a), as being unpatentable over Seal et al. (U.S. 5,583,804, "Seal" hereinafter). Applicants respectfully traverse the rejections for at least the reasons set forth below.

In response to the Response to Arguments stated in the Office Action, claims 1-2 and 9-10 are cancelled from the application. Limitations of claim 1 and 9 are respectively introduced into claims 3 and 11, which emphasizes that the selector selects one of the special and general register banks and outputting a selected N-bit result from the selected register bank **in according to a class signal received by the selector**, wherein the selected N-bit result and a N-bit data form a 2N-bit addition operand. Therefore, the selection takes place at the run-time.

Furthermore, only one accumulator is required in the application for performing accumulate operation upon the 2N-bit multiplied result and the 2N-bit addition operand and outputting a 2N-bit accumulated result (N*N+2N→2N). The architecture is different from that disclosed in the Seal reference, which stated that "high-precision instructions select and read from the registers in parallel to get the operands (see Seal Fig.3), while the low-precision instructions select and read from three registers in parallel to get the operands (see Seal Fig.2)." Instead of using the registers selected for high-precision instructions or low-precision instructions and applied to different accumulators, the only one accumulator in the invention performs fixed operation (N*N+2N→2N). By a class signal received by the selector, one N-bit addition operand for the "2N-bit addition operand" claimed is from the selection between output of the special register bank and the output of the general register bank, for the desired high-precision instructions or the low-precision instructions.

Consequently, the combination of Seal and the alleged well-known art does not render claims 1 and 9 obvious, and the rejection should be withdrawn.

Because independent claims 3 and 11 is allowable over the prior art of record, their respective dependent claims 4-8 and 12-16 are allowable as a matter of law, for at least the reason that these dependent claims contain all features of their respective independent claims 3 and 11.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 3-8 and 11-16 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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Date: 6/14/2004

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